## We claim:

- 1 1. A method for manufacturing a PIN diode, comprising the following steps:
- 2 forming a p-area on a first surface of a substrate;
- forming an n-area on the first surface of the substrate spaced apart from the p-
- 4 area;
- forming an intermediate area on the first surface of the substrate between the p-
- 6 area and the n-area, wherein a doping concentration of the intermediate area is lower
- 7 than a doping concentration of the p-area and lower than a doping concentration of the
- 8 n-area;
- 9 forming a first electrically conductive member on a side of the p-area, which
- 10 faces away from the intermediate area; and
  - forming a second electrically conductive member on a side of the n-area,
  - which faces away from the intermediate area.
    - 1 2. The method in accordance with claim 1, comprising the following steps:
  - 2 providing the substrate and a device substrate; and
  - 3 wafer-bonding of the substrate and the device substrate, wherein the p-area, the
- n-area and the intermediate area are formed in the device substrate and insulated
  - 5 against the substrate.
  - 1 3. The method in accordance with claim 2, comprising the following steps:
  - 2 forming a trench in a section of the device substrate, which abuts on the
  - 3 intermediate area, wherein the trench extends from a surface of the device substrate,
  - 4 which faces away from the substrate, to a surface of the device substrate, which is
  - 5 opposite to the substrate; and
  - 6 filling the trench with an insulating material.
  - 1 4. The method in accordance with claim 3, wherein the trench is further formed
  - 2 in sections of the device substrate, which abut on the p-area and on the n-area.

- 1 5. The method in accordance with claim 2, wherein the p-area or the n-area,
- 2 respectively, is formed by
- forming a trench in the device substrate and filling the same with p-doped or n-
- 4 doped polysilicon, respectively, or by
- 5 implanting of p-material or n-material, respectively, in predetermined areas of
- 6 the device substrate, or by
- 7 forming a trench in the device substrate, introducing of p-material or n-
- 8 material, respectively, into the same and diffusing of the introduced material into the
- 9 areas of the device substrate surrounding the trench.
- 1 6. The method in accordance with claim 1, further comprising the following step:
- forming an insulating layer above the surface of the p-area, the n-area, and the
- 3 intermediate area, which faces away from the-first surface of the substrate.
- 1 7. The method in accordance with claim 1, further comprising the following step:
- 2 forming of pads on the surfaces of the p-area and the n-area, which face away
- 3 from the first surface of the substrate.

- 1 8. A PIN diode comprising:
- 2 a p-area on a first surface of a substrate;
- an n-area on the first surface of the substrate;
- an intermediate area on the first surface of the substrate between the p-area and
- 5 the n-area, wherein a doping concentration of the intermediate area is lower than a
- 6 doping concentration of the p-area and lower than a doping concentration of the n-
- 7 area;
- 8 a first electrically conductive member, which is arranged on a side of the p-
- 9 area, which faces away from an intermediate area; and
- a second electrically conductive member, which is arranged on a side of the n-
- area, which faces away from the intermediate area.
- 1 9. The PIN diode in accordance with claim 8, having an insulating layer on the
- 2 substrate and a device substrate on the insulating layer, wherein the p-area, the n-area,
- 3 and the intermediate area are arranged in the device substrate.
- 1 10. The PIN diode in accordance with claim 8, comprising:
- a trench in a section of the device substrate, which abuts on the intermediate
- 3 area, wherein the trench extends from a surface of the device substrate, which faces
- 4 away from the substrate, to a surface of the device substrate, which is opposite to the
- 5 substrate, and wherein the trench is filled with an insulating material.
- 1 11. The PIN diode in accordance with claim 10, wherein the trench is arranged in
- 2 sections of the device substrate, which abut on the p-area and on the n-area.
- 1 12. The PIN diode in accordance with claim 11, wherein a shape of the
- 2 intermediate area, which is determined by the trench, is essentially rectangular,
- 3 wherein the p-area and the n-area are arranged on two opposite sides of the
- 4 intermediate area.

- 1 13. The PIN diode in accordance with claim 11, wherein the shape of the
- 2 intermediate area, which is determined by the trench, is essentially rectangular and, in
- addition, a further n-area or a further p-area is provided, wherein the n-area and the
- 4 further n-area or the p-area and the further p-area, respectively, are arranged on
- 5 opposite sides of the intermediate area and the p-area or the n-area, respectively, are
- 6 arranged between the n-area and the further n-area or between the p-area and the
- further p-area, respectively, and being spaced apart from the same in the intermediate
- 8 area.
- 1 14. The PIN diode in accordance with claim 12, wherein at least either the p-area
- 2 or the n-area extend along a whole width of the intermediate area.
- 1 15. The PIN diode in accordance with claim 11, wherein a shape of the
- 2 intermediate area, which is determined by the trench is essentially trapezoidal, wherein
- 3 the p-area extends along one of the parallel sides of the intermediate area, and wherein
- 4 the n-area extends along the other of the parallel sides of the intermediate area.
- 1 16. The PIN diode in accordance with claim 11, wherein a shape of the
- 2 intermediate area, which is determined by the trench, is essentially circular, wherein
- 3 either the p-area or the n-area is arranged in the shape of a circle along the edge of the
- 4 intermediate area, wherein the n-area or the p-area, respectively, is essentially
- 5 arranged in the center of the intermediate area and wherein the second electrically
- 6 conductive member or the first electrically conductive member, respectively, is
- 7 arranged in its center.
- 1 17. The PIN diode in accordance with claim 8, further comprising:
- a further insulating layer, which covers surfaces of the p-area, the n-area, and
- 3 the intermediate area, which face away from the substrate.

- 1 18. The PIN diode in accordance with claim 8, wherein a first pad is conductively
- 2 connected to the p-area and a second pad is conductively connected to the n-area,
- 3 wherein the two pads are arranged at the surfaces of the p-area and the n-area, which
- 4 face away from the first surface of the substrate.
- 1 19. The PIN diode in accordance with claim 8, wherein the distance between the p-
- 2 area and the n-area is more than 30  $\mu$ m.